Hall Ticket Number:

Code No. : 22658

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

M.E. (E.C.E.) II-Semester Main Examinations, September-2022

Mixed Signal IC Design

(Embedded Systems & VLSI Design)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	What is the need of mixed signal circuit in IC design?	2	1	2	3
2.	Why switched capacitor circuit is required in mixed signal IC design?	2	1	2	3
3.	What is the sampling and amplification mode of operation in switched capacitor circuit?	2	1	1, 3	3
4.	Define the input off-set voltage of a comparator?	2	1	1, 3	3
5.	What is the role of sample and hold circuit in converters?	2	1	1, 3	3
6.	Define the LSB and quantization error voltages in converters?	2	1	1, 3	3
7.	Define the quantization and sampling process of the signal?	2	1	1, 3	3
8.	What is the Nyquist and over sampling rate of the signal?	2	1	1, 3	3
9.	Compare the advantages of over sampling converters with Nyquist rate converters.	2	2	1, 3	3
10.	Deduce the relation of capture and locking range of the PLL in terms of LPF cutoff frequency?	2	3	1, 3	3
	Part-B (5 × 8 = 40 Marks)				
11. a)	Explain briefly about the mixed signal functions in IC design?	4	2	2	3
b)	Discuss the role of ADC and DAC in mixed signal IC design.	4	2	2	3
12. a)	Derive the gain expression of parasitic-insensitive integrator with waveforms.	4	3	1, 3	3
b)	Design the latch-based comparator and explain its working principle.	4	4	1, 3	3,4
13. a)	Design the sample and hold circuit with clock feed through cancellation.	4	4	2	3,4
b)	Explain the problems of clock feed through and charge injection in sample and hold circuits.	4	2	1, 3	3

Contd... 2

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14. a)	Develop the cyclic 4-bit ADC and explain its operation.	4	3	1, 3	3
b)	Design the inverted R-2R ladder type 3-bit DAC circuit with one example.	4	4	1, 3	3,4
15. a)	Describe the architecture of over sampling ADC circuit.	4	2	1, 3	3
b)	Explain the operation of digital PLL with diagram.	4	2	1, 3	3
16. a)	Derive the expression of signal to quantization noise of a converter?	4	3	1, 3	3
b)	Explain the operation of a switched capacitor-based amplitude modulator.	4	2	1, 3	3
17.	Answer any ***two*** of the following:				
a)	Develop the diode bridge based sample and hold circuit?	4	3	1, 3	3
b)	Design the 4-bit pipelined ADC and explain its operation?	4	4	1, 3	3,4
c)	Describe the architecture of over sampling DAC circuit.	4	2	1, 3	3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	37.5%
iii)	Blooms Taxonomy Level – 3 & 4	42.5%

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